Xilinx Day in Mons

Xilinx Technical Seminar

SILICA
The Engineers of Distribution

Agenda

June 10 2014

One day to discover
Xilinx's All programmable Technologies
FPGA & SoC design with demos

University of Mons
Faculty of Engineering
31 Bd Dolez Mons 7000 Belgium

Free admission - Ticket registration email to:
Johan.Deben@silica.com

9.00 – 9.10	Welcome
9.10 – 9.40	Xilinx – 30 years of Innovation
9.40 – 10.10	Artix/Kintex/Virtex & Ultrascale FPGAs This session will focus on giving an overview of the actual generation of Xilinx FPGAs and will give an introduction into new technologies (20 and 16 nm)
10.10 – 10.40	Zynq SOC In this session you will see an overview about the Zynq-7000 All Programmable SoC its hardware architecture, tools, and the comprehensive ecosystem of software solutions, tools.
10.40 – 11.00	Break & Demo's
11.00 – 11.30	Vivado Tools This session will focus on the Vivado® Design Suite which is a SoC-strength, IP- and system-centric, next generation development environment and outline the overall productivity, ease-of-use, and system level integration capabilities.
11.30 – 12.00	HW Tools for SOC designs This session will focus on HW tools that are available to help you creating Zynq™ SOC designs These include an overview of available evaluation boards and SOM Modules
12.00 - 13.00	Lunch & Demo's
13.00 - 13.45	How to Accelerate OpenCV applications using Vivado HLS This session will show how to accelerate existing OpenCV applications by leveraging the heterogeneous processing power of Zynq. Using the Vivado High Level Synthesis tool allows us to perform real-time video processing on an embedded device, with a very low power budget.
13.45 - 14.30	Smarter Vision: Solutions for your video applications This session shows IP and solutions for video applications in different application areas
14.30 - 15.00	Break & Demo's
15.00 - 16.00	Smarter Systems This session focusses on different topics where Xilinx can provide solutions These include topics like Industrial Communication Busses, Functional Safety, SDR, Motor Control
16.00 - 16.10	Closing

Organisation
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